REMARKS

Claims 21-25 are pending in the present application. Claims 26-42 have been canceled as being non-elected claims. Applicant respectfully reserves the right to file a divisional application including the non-elected claims.

Priority

Applicant respectfully notes the Examiner's acknowledgment of the Claim for Priority under 35 U.S.C. 119, and receipt of the certified copy of the priority document. Applicant confirms that Japanese priority application 216851/2000 corresponds to the present application.

Drawings

Applicant notes the Examiner's approval of the proposed drawing corrections filed on April 22, 2003. Accordingly, five (5) drawing Replacement Sheets incorporating the approved drawing corrections are enclosed herewith. **The Examiner is respectfully requested to acknowledge receipt and approval of the drawing Replacement Sheets.**

Claim Rejections-35 U.S.C. 103

Claims 21-23 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Peeters et al. reference (U.S. Patent No. 6,393,592) in view of the Kato

reference (Japanese patent publication 61-016615). This rejection is respectfully traversed for the following reasons.

As noted above, the Examiner has relied upon the combination of the Peeters et al. and Kato references. However, Applicant respectfully submits that the prior art as relied upon by the Examiner taken singularly or together does not disclose or make obvious all the features as set forth in claim 21.

Enclosed is an Explanatory Drawing (Fig. 1) provided to assist in emphasizing the differences between the semiconductor device of the present invention and the teachings of the combined prior art. In the Explanatory Drawing, symbol tx indicates the access time of macro cell 101, that is the required time from when clock TCLK is supplied to terminal CLK (that is, when signal level of terminal D is read) until signal Q is output from terminal Q of macro cell 101. Symbol t2 indicates the wiring delay time of the third path, that is the time required from when signal Q is output from macro cell 101 until the signal Q reaches pad 109. Furthermore, symbol t3 indicates the wiring delay time of the fourth path, that is the required time from when the test clock TCLK is supplied to the terminal CLK until the test clock TCLK reaches pad 110. Here, in the present invention, delay time t2 and t3 are set up to be substantially equal as described on page 8, lines 2-4 of the present application. Accordingly, the present invention can measure the access time tx exactly by measuring the time difference from when pad 110 outputs test clock TCLK until pad 109 outputs signal Q, as described on page 8, line 5 through to page 9, line 15 of the present application.

In contrast, the circuit in Fig. 3 of the Kato reference includes a signal path for transferring a clock signal via delay circuit 12 and buffer gate 5 to output terminal 7 of the circuit. The delay time of delay circuit 12 is set up to be equal to the access time of flip flop 3 (that is, the delay time from when flip flop 3 reads input data D at terminal 9 until the flip flop outputs data Q from terminal 10 of the flip flop). Therefore, in the Fig. 3 circuit of the Kato reference, the delay time from when the clock signal is supplied to clock terminal 8 of the flip flop until the clock signal reaches output terminal 7 of the circuit (this delay time corresponds to t3 in the Explanatory Drawing), is equal to the sum of the access time of flip flop 3 (this access time corresponds to tx of the Explanatory Drawing) and the delay time from terminal 10 of flop flop 3 to output terminal 6 of the circuit (this delay time corresponds to t2 of the Explanatory Drawing). Again, this is because the delay time of delay circuit 12 is set up to be equal to that of the access time of flip flop 3.

Accordingly, in the Fig. 3 circuit of the Kato reference, the delay times that correspond to t2 and t3 in the Explanatory Drawing, **are not set up to be substantially equal**. That is, the signal path from clock terminal 8 of flip flop 3 in Fig. 3 of the Kato reference to output terminal 7 of the circuit (fourth signal path), and the signal path from terminal 10 of flip flop 3 to output terminal 6 of the circuit (third signal path), are not set to be substantially the same, because delay circuit 12 is placed along the signal path between terminal 8 of flip flop 3 and output terminal 7 of the circuit. In other words, the Fig. 3 circuit of the Kato reference does not have third and fourth signal paths set so

that wiring delay times of the third and fourth signal paths are substantially equal, as featured in claim 21. The Fig. 3 circuit of the Kato reference therefore cannot measure access time tx, because data Q and the clock signal are output simultaneously.

As noted above, the present invention has as an object to measure the access time exactly. In contrast, the circuit of the Kato reference as relied upon by the Examiner has as an object to make data Q and the clock signal be output simultaneously. Accordingly, the objects of the present invention and that of the Kato reference are clearly different from each other. The Peeters et al. reference as taken with the Kato reference therefore clearly fail to disclose or make obvious third and fourth signal paths that are formed so that wiring delay time of third and fourth signal paths are substantially equal, as featured in claim 21. Applicant therefore respectfully submits that the semiconductor device of claim 21 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection of claims 21-23 is improper for at least these reasons.

Claims 24 and 25 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Peeters et al. reference in view of the Kato reference, in further view of the Kapur et al. reference (U.S. Patent No. 6,615,380). Applicant respectfully submits that the Kapur et al. reference as relied upon by the Examiner does not overcome the above noted deficiencies of the primarily relied upon prior art. Applicant therefore respectfully submits that claims 24 and 25 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and

that this rejection is improper for at least these reasons.

Conclusion

The Examiner is respectfully requested to enter the current Amendment. Since only non-elected claims 26-42 have been canceled, and since pending claims 21-25 have not been amended, entry and consideration of this Amendment should not be an undue burden.

The Examiner is further respectfully requested to reconsider and withdraw the corresponding rejections, and to pass the claims of the present application to issue, for at least the above reasons.

In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (703) 715-0870 in the Washington, D.C. area, to discuss these matters.

Pursuant to the provisions of 37 C.F.R. 1.17 and 1.136(a), the Applicant hereby petitions for an extension of one (1) month to February 28, 2004, for the period in which to file a response to the outstanding Office Action. The required fee of $110.00 should be charged to Deposit Account No. 50-0238.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

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Enclosures: Five (5) Drawing Replacement Sheets
Explanatory Drawing Fig. 1